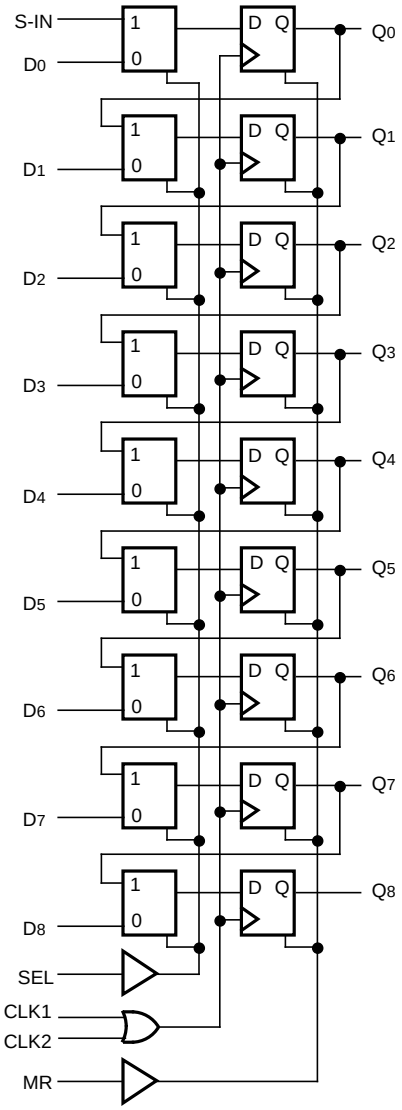
查询SY100E142供应商

FEATURES

- 700MHz min. shift frequency
- Extended 100E VEE range of –4.2V to –5.5V
- 9 bits wide for byte-parity applications
- Asynchronous Master Reset
- Dual clocks
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E142
- Available in 28-pin PLCC package

BLOCK DIAGRAM



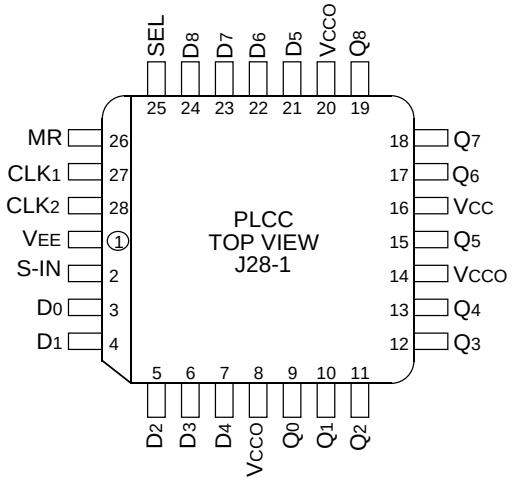
DESCRIPTION

The SY10/100E142 are high-speed 9-bit shift registers designed for use in new, high-performance ECL systems. The E142 can accept serial or parallel data to be shifted out in one direction as both serial and parallel outputs. The nine inputs, D0-D8, accept parallel input data, while S-IN accepts serial input data.

The SEL (Select) control pin serves to determine the mode of operation, either SHIFT or LOAD. The shift direction is from bit 0 to bit 8. The input data has to meet the set-up time before being clocked into the nine input registers on the rising edge of CLK1 or CLK2. Shifting is also performed on the rising edge of either CLK1 or CLK2. The MR (Master Reset) control signal asynchronously resets all nine registers to a logic LOW when a logic HIGH is applied to MR.

The E142 is designed for applications such as diagnostic scan registers, parallel-to-serial conversions and is also suitable for byte-wide parity.

PIN CONFIGURATION



PIN NAMES

Pin	Function
D0-D8	Parallel Data Inputs
S-IN	Serial Data Input
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q0-Q8	Data Outputs
VCCO	VCC to Output

TRUTH TABLE

SEL	MODE
L	LOAD
H	SHIFT

DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	µA	—
I_{EE}	Power Supply Current										mA	—
	10E	—	120	145	—	120	145	—	120	145		
	100E	—	120	145	—	120	145	—	138	165		

AC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CCO} = GND

Symbol	Parameter	T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
f_{SHIFT}	Max. Shift Frequency	700	900	—	700	900	—	700	900	—	MHz	—
t_{PLH} t_{PHL}	Propagation Delay to Output										ps	—
	CLK	600	800	1000	600	800	1000	600	800	1000		
	MR	600	800	1000	600	800	1000	600	800	1000		
t_S	Set-up Time										ps	—
	D	50	–100	—	50	–100	—	50	–100	—		
	SEL	300	150	—	300	150	—	300	150	—		
t_H	Hold Time										ps	—
	D	300	100	—	300	100	—	300	100	—		
	SEL	75	–150	—	75	–150	—	75	–150	—		
t_{RR}	Reset Recovery Time	900	700	—	900	700	—	900	700	—	ps	—
t_{PW}	Minimum Pulse Width CLK, MR	400	—	—	400	—	—	400	—	—	ps	—
t_{skew}	Within-Device Skew	—	75	—	—	75	—	—	75	—	ps	1
t_r t_f	Rise/Fall Time 20% to 80%	300	525	800	300	525	800	300	525	800	ps	—

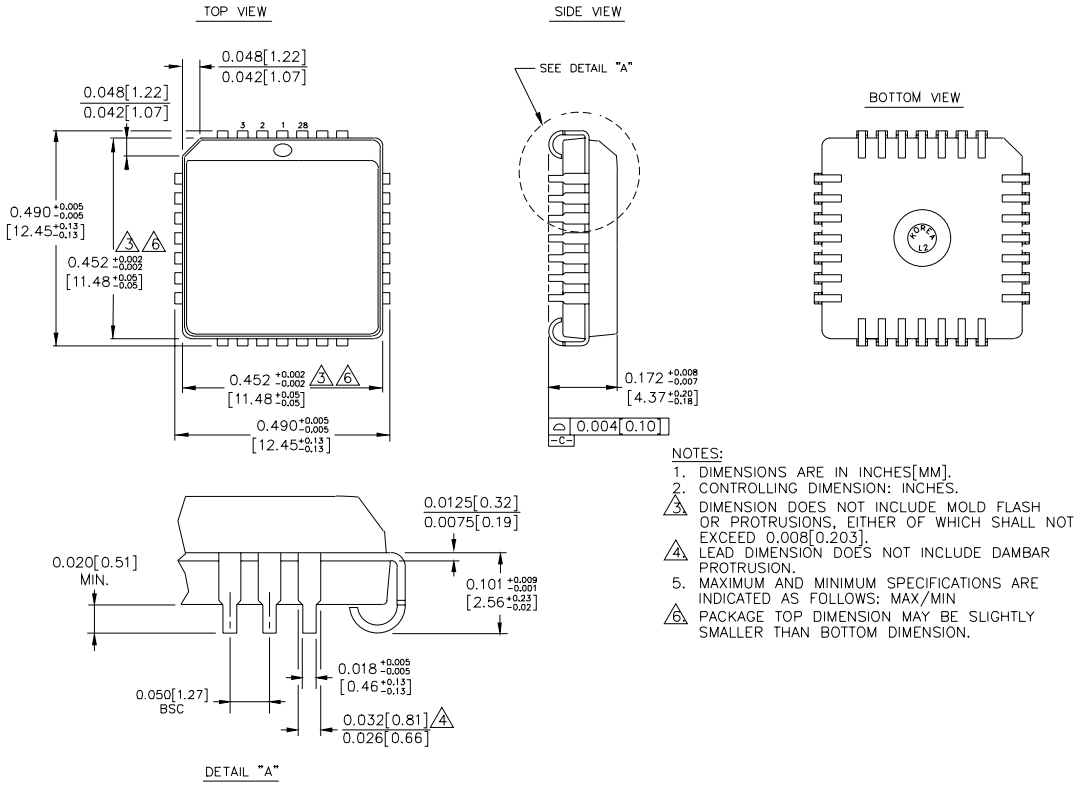
NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E142JC	J28-1	Commercial
SY10E142JCTR	J28-1	Commercial
SY100E142JC	J28-1	Commercial
SY100E142JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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